SY88053AL

3.3V, 12.5Gbps Limiting Post Amplifier with Programmable Decision Threshold

General Description

The SY88053AL, limiting post amplifier is designed for use in fiber-optic receivers for applications up to 12.5Gbps. It features a decision threshold control that can be used for offset compensation or to optimize the Bit Error Rate (BER) in noisy applications as WDM where optical amplifiers such as EDFAs and Raman amplifier are used. This device connects to typical transimpedance amplifiers (TIAs). The signal from TIAs can contain significant amounts of noise unevenly distributed between its top and bottom rails due to the Amplified Spontaneous Emission (ASE) noise generated by the optical amplifiers. In order to optimize the BER in such noisy conditions, the decision threshold between bit 1 and bit 0 needs to be moved to the rail that contains less noise. An external voltage applied at the VTHP pin on the SY88053AL will move the crossing point up and down, from 20% to 80%, to achieve the best BER.

The SY88053AL operates from a single +3.3V power supply, over temperatures ranging from –40°C to +85°C, and can detect and amplify signals up to 12.5Gbps and amplitude as low as 15mV$_{PP}$.

The SY88053AL generates a Loss-of-Signal (LOS) open-collector TTL output. A programmable Loss-of-Signal level set pin (LOS$_{LVL}$) sets the sensitivity of the input amplitude detection. LOS asserts high if the input amplitude falls below the threshold set by LOS$_{LVL}$ and de-asserts low otherwise. The enable input (/EN) de-asserts the true output signal without removing the input signal. The LOS output can be fed back to the /EN input to implement the squelch function that maintains output stability under a loss-of-signal condition.

All support documentation can be found on Micrel's web site at: www.micrel.com.

Features

- Single 3.3V power supply
- Up to 12.5Gbps operation
- Programmable Decision Threshold
- Low-noise CML data outputs
- TTL /EN input
- Programmable LOS level (LOS$_{LVL}$)
- Available in a tiny 3mm x 3mm MLF® package

Applications

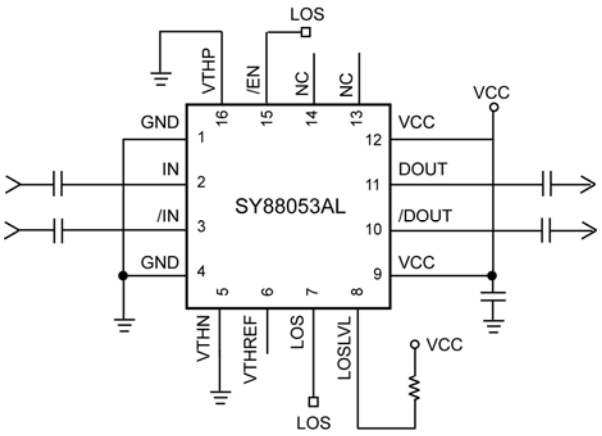
- WDM Systems
- 10xGigabit Ethernet, 8xFibre Channel
- SONET/SDH:OC192 – STM64
- Low-gain TIA interface

Markets

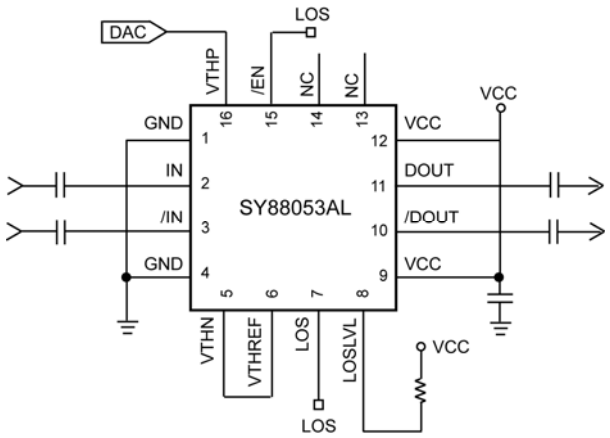
- Datacom/telecom
- Optical transceiver

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Typical Application Circuit



Fixed Decision Threshold



Programmable Decision Threshold

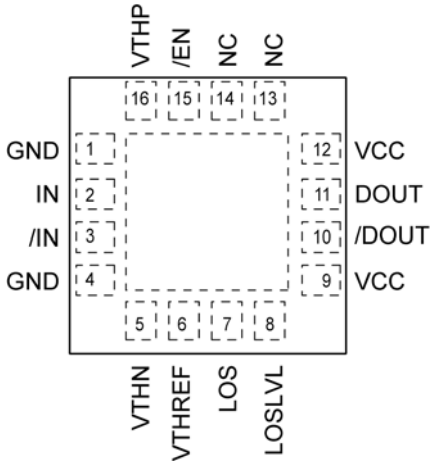
Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY88053ALMG	MLF-16	Industrial	053A with Pb-Free bar line indicator	NiPdAu Pb-Free
SY88053ALMGTR(1)	MLF16	Industrial	053A with Pb-Free bar line indicator	NiPdAu Pb-Free

Note:

1. Tape and Reel.

Pin Configuration



16-Pin (3mm x 3mm) MLF® (MLF-16)

hbwhelp@micrel.com or (408) 955-1690

Pin Description

Pin Number	Pin Name	Type	Pin Function
2, 3	DIN, /DIN	Data Input	Differential data inputs. Each input is internally terminated to approximately VCC – 1.3V by a 50Ω resistor. AC-Couple input signals.
5	VTHN	DC Input	Tie this pin to pin 6 (VTHREF) and apply a DC voltage on pin 16 (VTHP) for signal crossing adjustment. Connect to ground if no crossing adjustment is needed.
6	VTHREF	DC Output	1.25V Reference voltage (referenced to ground) for decision threshold adjustment.
7	LOS	Open-collector TTL output	Loss-of-Signal: asserts high when the data input amplitude falls below the threshold set by LOS_{LVL}.
8	LOSLVL	DC Input	Loss-of-Signal Level Set. A resistor from this pin to V_{CC} sets the threshold for the data input amplitude at which LOS will be asserted.
10, 11	/DOUT, DOUT	CML Output	Differential data outputs. Unused output should be terminated 50Ω-to-VCC.
13, 14	NC, NC	No Connection	Unused pins.
15	/EN	TTL Input	/Enable: This input enables the outputs when it is LOW. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open.
16	VTHP	DC Input	Apply a DC voltage from 0 to 2.4V to adjust the signal crossing level when pin 5 (VTHN) is tied to pin 6 (VTHREF). 1.25V sets the crossing close to 50%. Connect to ground if no crossing adjustment is needed.
1,4	GND	Ground	Device ground. Exposed pad must be soldered (or equivalent) to the same potential as the ground pins.
9, 12	VCC	Power Supply	Positive power supply. Bypass with 0.1µF||0.01µF low ESR capacitors. 0.01µF capacitors should be as close as possible to VCC pins.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... 0V to +4.0V
Input Voltage (DIN, /DIN) .....(V_{CC}-1.0V) to (V_{CC}+0.5V)
Output Current (I_{OUT}) ..... ±25mA
EN Voltage ..... 0 to V_{CC}
LOS_{LVL} Voltage ..... V_{CC}-1.3V to V_{CC}
Lead Temperature (soldering, 20sec.) ..... 260°C
Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... +3.0V to +3.6V
Ambient Temperature (T_A)..... –40°C to +85°C
Package Thermal Resistance[3]
MLF®
(θ_{JA}) Still-air ..... 60°C/W
(ψ_{JB})..... 33°C/W

DC Electrical Characteristics

V_{CC} = 3.0 to 3.6V; T_A = –40°C to +85°C, typical values at V_{CC} = 3.3V, T_A = 25°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{CC}	Power Supply Current	Note 4		50	70	mA
LOS_{LVL}	LOS_{LVL} Voltage		V_{CC} -1.3		V_{CC}	V
V_{OH}	DOUT, /DOUT HIGH Voltage		V_{CC}-0.020	V_{CC}-0.005	V_{CC}	V
V_{OL}	DOUT, /DOUT LOW Voltage		V_{CC}-0.400	V_{CC}-0.350	V_{CC}-0.300	V
V_{OFFSET}	Differential Output Offset	VTHP and VTHN tied to GND			±80	mV
V_{THREF}	Decision Threshold Reference Voltage			1.25		V
Z_0	Single-Ended Output Impedance		45	50	55	Ω
Z_I	Single-Ended Input Impedance		45	50	55	Ω

TTL DC Electrical Characteristics

V_{CC} = 3.0 to 3.6V; T_A = –40°C to +85°C, typical values at V_{CC} = 3.3V, T_A = 25°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Output Signal Crossing Range Lower Limit	Note 5			20	%
	Output Signal Crossing Range Upper Limit		80			%
V_{IH}	/EN Input HIGH Voltage		2.0			V
V_{IL}	/EN Input LOW Voltage				0.8	V
I_{IH}	/EN Input HIGH Current	V_{IN} = 2.7V V_{IN} = V_{CC}			20 100	µA µA
I_{IL}	/EN Input LOW Current	V_{IN} = 0.5V	-0.3			mA
V_{OH}	LOS Output HIGH Level	Sourcing 100µA	2.4			V
V_{OL}	LOS Output LOW Level	Sinking 2mA			0.5	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package Thermal Resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. ψ_{JB} uses a 4-layer and θ_{JA} in still air unless otherwise stated.
4. VTHN and VTHP are both at GND potential and with outputs Q and /Q loaded and with the device enabled.
5. VTHN connected to VTHREF and DC voltage between 0V and 2.4V applied to VTHP. Input at DIN is between 15mVpp to 60mVpp. See Figure on page 7

AC Electrical Characteristics

V_{CC} = 3.0 to 3.6V; R_{Load} = 50Ω to V_{CC}; T_A = –40°C to +85°C, typical values at V_{CC} = 3.3V, T_A = 25°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
t_r, t_f	Output Rise/Fall Time (20% to 80%)	Note 6		25	35	ps
t_{JITTER}	Deterministic Random	Note 7 Note 8		10 1		ps_{PP} ps_{RMS}
V_{ID}	Differential Input Voltage Swing		15		1800	mV_{PP}
V_{OD}	Differential Output Voltage Swing	Note 6	600	700	800	mV_{PP}
T_{OFF}	LOS Release Time	Note 11		100	500	ns
T_{ON}	LOS Assert Time	Note 11		100	500	ns
LOS_{AL}	Low LOS Assert Level	R_{LOSLVL} = 10kΩ, Note 9	5	14		mV_{PP}
LOS_{DL}	Low LOS De-assert Level	R_{LOSLVL} = 10kΩ, Note 9		20	25	mV_{PP}
HSY_L	Low LOS Hysteresis	R_{LOSLVL} = 10kΩ, Note 10	2	3.0	6	dB
LOS_{AM}	Medium LOS Assert Level	R_{LOSLVL} = 5kΩ, Note 9	10	21		mV_{PP}
LOS_{DM}	Medium LOS De-assert Level	R_{LOSLVL} = 5kΩ, Note 9		30	40	mV_{PP}
HSY_M	Medium LOS Hysteresis	R_{LOSLVL} = 5kΩ, Note 10	2	3.0	6	dB
LOS_{AH}	High LOS Assert Level	R_{LOSLVL} = 100Ω, Note 9	35	55		mV_{PP}
LOS_{DH}	High LOS De-assert Level	R_{LOSLVL} = 100Ω, Note 9		76	85	mV_{PP}
HSY_H	High LOS Hysteresis	R_{LOSLVL} = 100Ω, Note 10	2	3.0	6	dB
B_{-3dB}	3dB Bandwidth			10		GHz
$A_{V(Diff)}$	Differential Voltage Gain			38		dB
S_{21}	Single-Ended Small-Signal Gain		26	32		dB

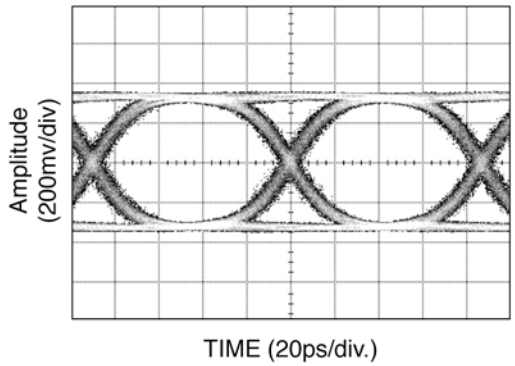
Notes:

6. Amplifier in limiting mode. Input is a 200MHz square wave.
7. Deterministic jitter measured using 10 Gbps K28.5 pattern, V_{ID} = 60mV_{PP}.
8. Random jitter measured using 10Gbps K28.7 pattern, V_{ID} = 60mV_{PP}.
9. See “Typical Operating Characteristics” for a graph showing how to choose a particular R_{LOSLVL} for a particular LOS assert and its associated de-assert amplitude.
10. This specification defines electrical hysteresis as 20log (LOS De-Assert/LOS Assert). The ratio between optical hysteresis and electrical hysteresis is found to vary between 1.5 and 2 depending upon the level of received optical power and ROSA characteristics. Based on that ratio, the optical hysteresis corresponding to the electrical hysteresis range 1dB-4.5 dB, shown in the AC characteristics table, will be 0.5dB-3dB Optical Hysteresis.
11. In real world applications, the LOS Release/Assert time can be strongly influenced by the RC time constant of the AC-coupling cap and the 50Ω input termination. To keep this time low, use a decoupling cap with the lowest value that is allowed by the data rate and the number of consecutive identical bits in the application (typical values are in the range of 0.001µF to 1.0µF).

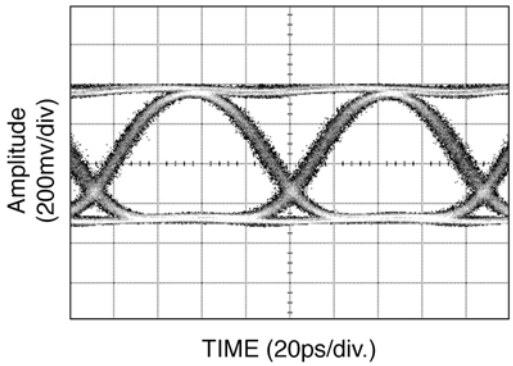
Typical Functional Characteristics

V_{CC} = 3.3V, T_A = 25°C, V_{THN} tied to V_{THREF}, R_L = 50Ω to V_{CC}-2V, unless otherwise stated.

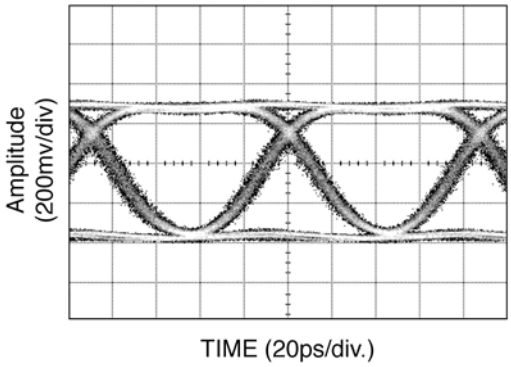
PRBS^{-23} Pattern, 11.3Gbps
V_{THP} = 1.25V, V_{IN} = 60mV$_{PP}$, Crossing = 50%



PRBS^{-23} Pattern, 11.3Gbps
V_{THP} = 1.45V, V_{IN} = 60mV$_{PP}$, Crossing = 20%



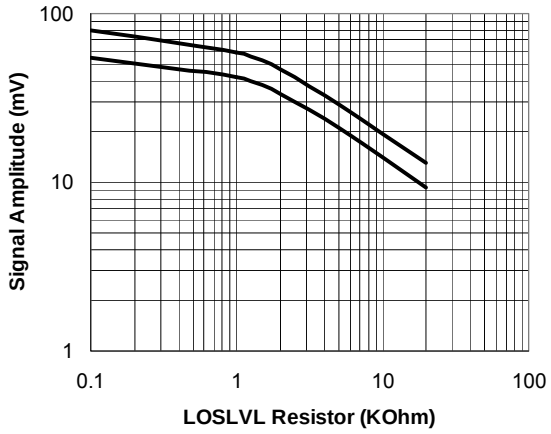
PRBS^{-23} Pattern, 11.3Gbps
V_{THP} = 1.05V, V_{IN} = 60mV$_{PP}$, Crossing = 80%



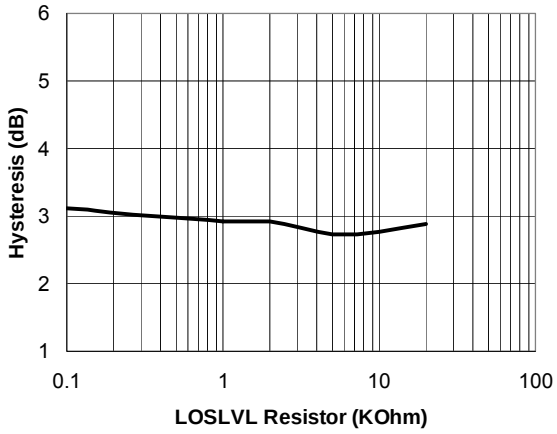
Typical Operating Characteristics

V_{CC} = 3.3V, T_A = 25°C, R_L = 50Ω to V_{CC}-2V, unless otherwise stated.

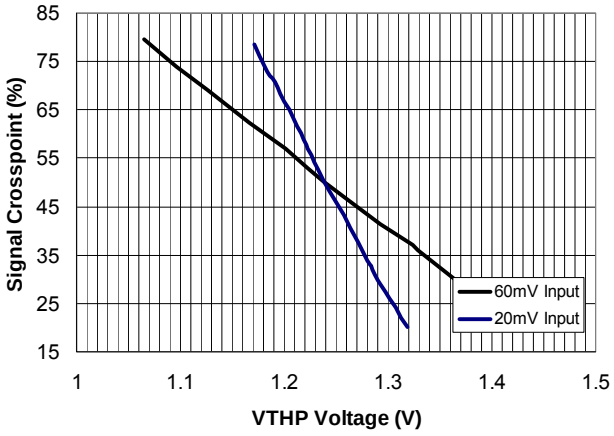
LOS Assert/De-Assert Levels



LOS Hysteresis



Crosspoint Adjustment



Detailed Description

The SY88053AL is a high-sensitivity limiting post amplifier that operates from a single +3.3V power supply over temperatures from –40°C to +85°C. Signals with data rates up to 12.5Gbps, and as small as 15mV$_{pp}$, can be amplified. Figure 1 shows the allowed input voltage swing. The SY88053AL generates a LOS output signal that can be fed back to /EN for output stability in the absence of a signal at the input. LOS$_{LVL}$ sets the sensitivity of the input amplitude detection. In the situations where the noise in not evenly distributed between the high and the low levels of the signal, such in links using EDFA amplifiers, the offset of the signal can be adjusted, using VTHN and VTHP pins to optimize the performance of the link.

Input Amplifier/Buffer

Figure 2 shows a simplified schematic of the input stage. The high-sensitivity of the input amplifier allows signals as small as 15mV$_{pp}$ to be detected and amplified. The input amplifier allows input signals as large as 1800mV$_{pp}$. Input signals are amplified with a typically 38dB differential voltage gain. Since it is a limiting amplifier, the SY88053AL outputs typically 700mV$_{pp}$ voltage-limited waveforms for input signals that are greater than 10mV$_{pp}$.

Output Buffer

The SY88053AL's CML output buffer is designed to drive 50Ω lines and is internally terminated with 50Ω to VCC. Figure 3 shows a schematic of the output stage.

Loss-of-Signal

The SY88053AL generates a chatter-free loss-of-signal (LOS) open-collector TTL output as shown in Figure 4. LOS is used to determine that the input amplitude is too small to be considered as a valid input. LOS asserts high if the input amplitude falls below the threshold set by LOSLVL and de-asserts low otherwise. LOS can be fed back to the enable (/EN) input to maintain output stability under a loss of signal condition. /EN de-asserts low the true output signal without removing the input signals. Typically, 3dB LOS hysteresis is provided to prevent chattering.

Loss-of-Signal-Level Set

A programmable LOS level set pin (LOS$_{LVL}$) sets the threshold of the input amplitude detection. Connecting an external resistor between V_{CC} and LOS$_{LVL}$ sets the voltage at LOS$_{LVL}$. This voltage ranges from V_{CC} to VCC-1.3V. The external resistor creates a voltage divider between V_{CC} and VCC-1.3V, as shown in Figure 5.

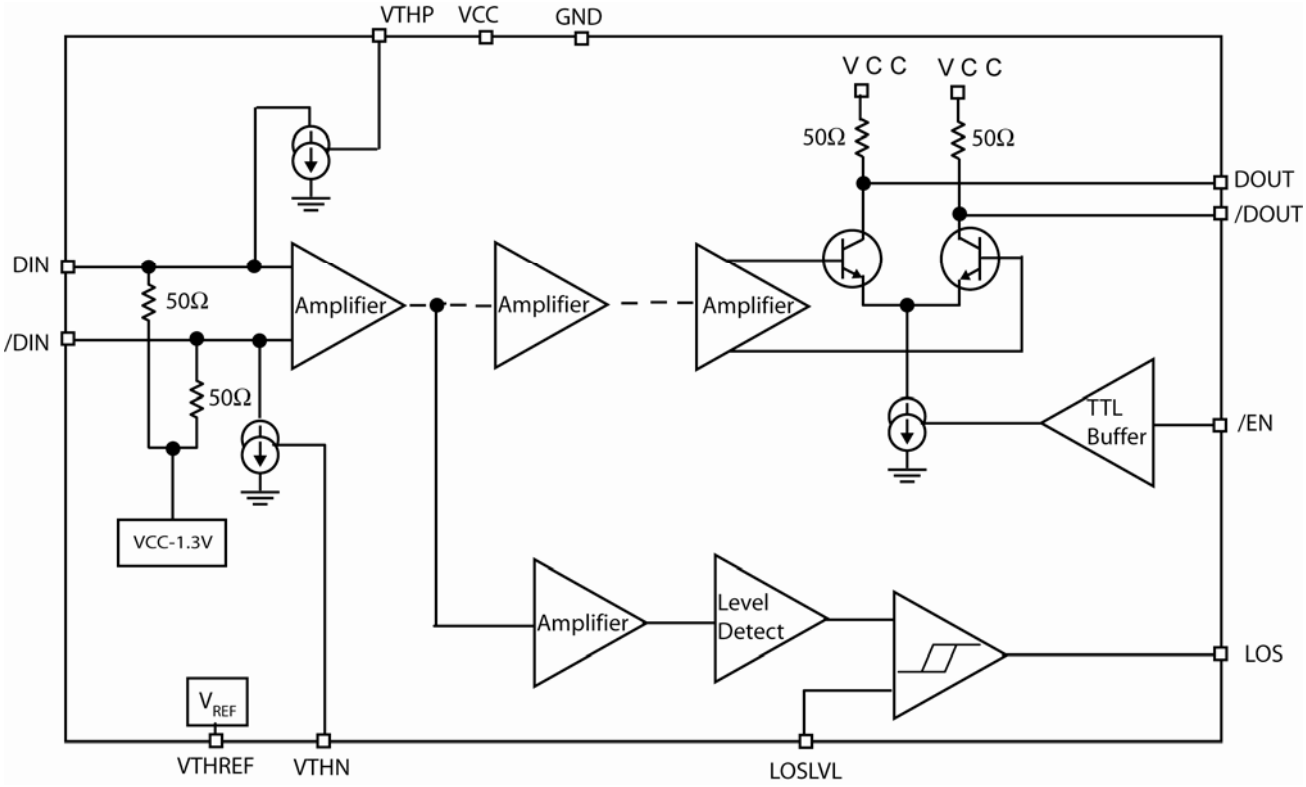
Hysteresis

The SY88053AL provides typically 3dB LOS electrical hysteresis, which is defined as 20log (VIN$_{LOS\text{-}Assert}$ / VIN$_{LOS\text{-}De\text{-}Assert}$). Since the relationship between the voltage out of the ROSA to optical power at its input is linear, the optical hysteresis will be typically half of the electrical hysteresis reported in the datasheet, but in practice the ratio between electrical and optical hysteresis is found to be within the range 1.5-1.8. Thus 3dB electrical hysteresis will correspond to an optical hysteresis within the range 1.7dB - 2dB.

Signal Crossing Adjustment

In order to optimize the BER of the optical link where the noise is unevenly distributed between the high and the low levels, the SY88053AL provides two pins for output signal crossing control. The output crossing can be adjusted by connecting pins VTHN and VTHREF together while applying a DC voltage at VTHP pin. By varying the DC signal at VTHP from 1V to 1.5V while the input signal to the post amplifier is less than 60mVpp, the crossing of the output signal will change from 20% to 80%. The output crossing is at 50% when VTHP = 1.25V. If the crossing control function is not needed, VTHN and VTHP should be connected to ground.

Functional Block Diagram



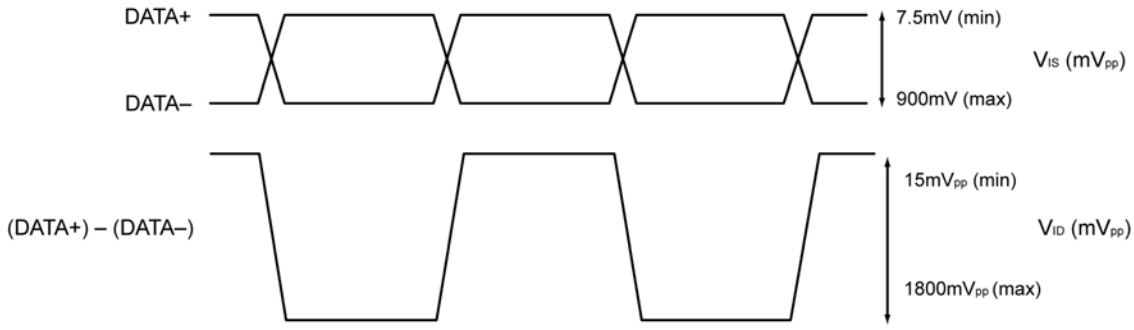


Figure 1. V_{IS} and V_{ID} Definition

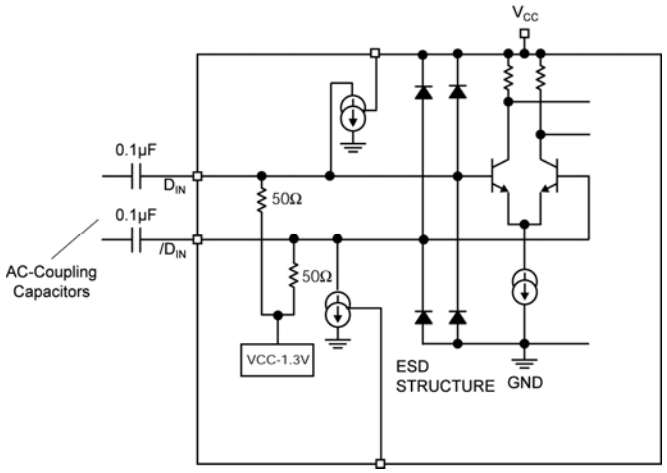


Figure 2. Input Structure

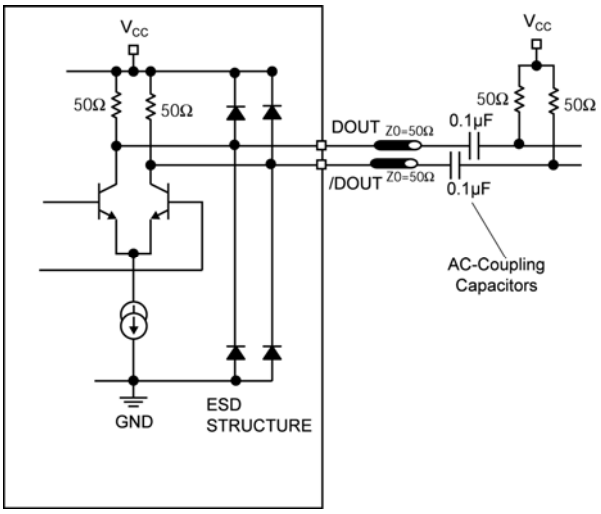


Figure 3. Output Structure

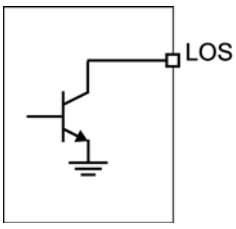


Figure 4. LOS Output Structure

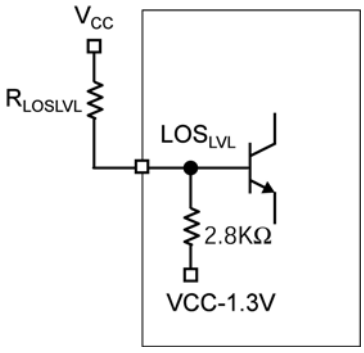
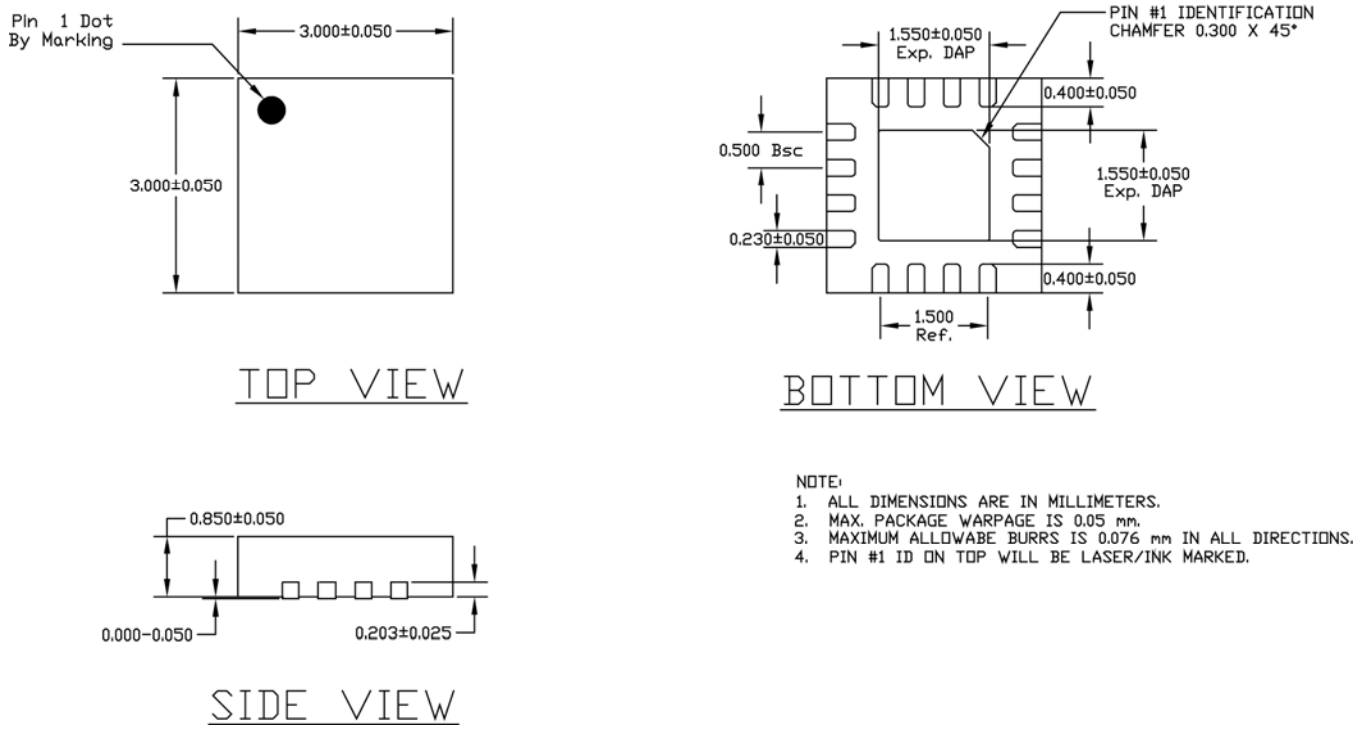


Figure 5. LOS_{LVL} Setting Circuit
Note: Recommended value for R_{LOSLVL} is 15kΩ or less.

Related Product and Support Documentation

Part Number	Function	Data Sheet Link
AN-45	Notes on Sensitivity and Hysteresis in Micrel Post Amplifiers	http://www.micrel.com/product-info/app_hints+notes.shtml

Package Information



16-Pin (3mm x 3mm) MLF® (MLF-16)

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